Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 15, with the following:

It is sometimes desired to achieve minimum cell rate assurance of each virtual channel (VC) of a virtual path (VP) and peak cell rate shaping of the virtual path and each virtual channel of the virtual path on condition of $\sum$ (VCMCR) $\leq$ VPPCR $\leq \sum$ (VCPCR) where $\sum$ (VCPCR) is the ~~peach~~ peak cell rate total value 20 of the virtual channels in the virtual path, $\sum$ (VCMCR) is the minimum cell rate total value of the virtual channels in the virtual path, and VPPCR is the peak cell [[rage]] rate of the virtual path. However, with a conventional shaper, if cell rate shaping is performed for each virtual path, then it is impossible to realize minimum cell rate assurance and peak cell rate shaping of each virtual channel in a virtual path.

Please replace the paragraph beginning on page 2, line 13, with the following:

~~It is an object~~ An aspect of the present invention ~~to provide~~ provides an ATM switch which realizes hierarchical shaping for each virtual channel and each virtual path with a simple configuration.

Please replace the paragraph beginning on page 2, line 16, with the following:

~~In order to attain the object described above, according to~~ In one aspect of the present invention, the output rate for each virtual channel is changed dynamically within a range from a minimum cell rate to a peak cell rate in accordance with a stored amount of cells by rate shaping for each virtual path.

Please replace the paragraph beginning on page 5, line 6, with the following:

The above ~~and other objects,~~ features and advantages of the present invention will become apparent from the following description and the appended claims, taken in conjunction with the accompanying drawings in which like parts or elements are denoted by like reference symbols.

Please replace the paragraph beginning on page 7, line 18, with the following:

Cells of each virtual channel are outputted at a rate equal to or ~~hither~~ higher than the minimum cell rate in accordance with a VC cell rate control signal representative of the cell storage amount in each of the output side circuit interfaces 3_0 to 3_N.